Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Two numbers A & B in Hex are given A= 85CA, B= 23C6 (10)

i. Find the Decimal equivalent of A & B

ii. Find the binary of A & B

iii. What is the sum of A& B in HEX

b) Write down the algorithm for BCD Addition. Find the sum of numbers 74998 and 38976 by BCD addition. Show the steps clearly. (5)

2 a Express f =AB + AC + C + AD + ABC + ABC in standard SOP form. (7)

b Using K map simplify the SOP function, and realize it using logic gates. (8)

$f(a,b,c,d) = \Sigma m (0,1,2,4,5,6)$, $d = \Sigma (3,7,14,15)$

3 a) Realize a XNOR circuit using NAND gate only. (6)

b) A logic circuit has our inputs A,B,C and D. A four bit input is fed with A as MSB and D as LSB. Design and implement a circuit such that the output is one when the input is more than or equal to decimal 6. (9)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Realize a 3 bit gray to binary decoder using PROM. Give all details. (7)

b) What is meant by race around condition? How it is eliminated. Illustrate with the help of necessary sketches. (8)

5 a) Convert a JK flipflop into a D flipflop, (7)

b) Design and implement a circuit for generating the sequence 2-5-7-3-0 (8)

6 a) Define the following (4)

(i) Fan out

(ii) Fan in

b) What is the difference between a latch and a flipflop. (3)

c) Design an asynchronous 3 bit up counter. Write complete truth table and excitation table. (8)

PART C

Answer any two full questions, each carries20 marks.

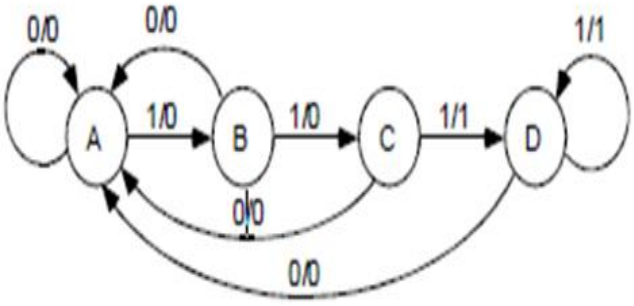
7 a) A register is to be designed, which provides all the following functions shift left, shift right, parallel in, parallel out, serial in, serial out, serial in parallel out and parallel in serial out. Draw the circuit for a 4 bit data (serial/parallel) and provide its working. (10)

b) Draw the Mealy machine for the given table. (10)

Present state	Next state, output	
	x=0	x=1
y_1 y_0	y_1 y_0 / z	y_1 y_0 / z
0 0	0 1, 0	1 0, 0
0 1	0 1, 1	1 0, 0
1 0	0 1, 0	1 1, 0
1 1	0 1, 0	1 1, 1

8 a) Draw the logic diagram of a Johnson counter. Why it is called a divide by 2N counter. Draw the neat diagram of clock and output waveforms of a 4 bit Johnson counter. (8)

b) Use the state reduction technique and implement the circuit for the given state diagram. (12)



9 a) Design a mealy machine to detect an input sequence10110. The system should be able to detect overlapped sequence. Also draw the state diagram (10)

b) Obtain a minimum row primitive flow table for the state table shown below. (10)

	X_1X_2				Z_1Z_2
	00	01	11	10	
1	(1)	7	-	4	11
2	(2)	5	-	4	01
3	-	7	(3)	11	10
4	2	-	3	(4)	00
5	6	(5)	9	-	11
6	(6)	7	-	11	01
7	1	(7)	14	-	10
8	(8)	12	-	4	01
9	-	7	(9)	13	01
10	-	7	(10)	4	10
11	8	-	10	(11)	00
12	6	(12)	9	-	11
13	8	-	14	(13)	11
14	-	12	(14)	11	00

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